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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,943	02/14/2002	Mark Champion	72708	3617

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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2676	8

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,943	CHAMPION ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-26* is/are rejected.

7)☒ Claim(s) *9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/6-14-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1A-B; Fig. 2; Figs. 3A-C; Fig. 4; Fig. 5; Fig. 6A-C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 18, 21, 23, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al.

a. Regarding claims 1 and 18, Reynolds **discloses** a data source (object receiver 51); a data destination (object builder 55); at least two memory devices

(RAM 45, RAM 46)(Fig. 3). Although, Reynolds does not disclose four memory devices but use of more than two memory devices is well known in the memory bank art for storage of more data. Reynolds **is silent about** a first order and a second order of providing and receiving data elements; data elements storage and retrieval in parallel from the memory devices. Takasugi **discloses** data elements storage and retrieval in parallel from the memory devices and **further discloses** a first order and second order of data elements processing and storage/retrieval in that high speed serial access in row and column direction is possible as well storage of data elements in multiple locations (...a memory comprised of a plurality of banks interleaving...different rows...high-speed...access in the column direction...by the memory...col. 4, lines 30-47; col. 5,lines 1-32). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made of modify the device as taught by Reynolds with the feature "high speed serial access in row and column direction using memory banks for storage and retrieval of data elements" as taught by Takasugi **because** it provides for quick access in row or column directions thus reducing data transfer latency. However, Reynolds-Takasugi combination **fails to disclose** storing data elements that are consecutive. Shreesha et al. **discloses** storing adjacent pixel elements (col. 4, lines 17-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi combination with the feature "storing adjacent pixel elements along one dimension of the image" as taught by

Shreeesha et al. **because** it allows blocks of image data to be fetched without latency.

b. Regarding claim 2, Reynolds **discloses** RAM memory elements 45 and 46 comprising an image buffer storage area (col. 5, lines 45-54).

c. Regarding claim 21, it is similar in scope to claim 1 above and is rejected under the same rationale.

d. Regarding claim 23, it is similar in scope to claim 1 above and is rejected under the same rationale.

e. Regarding claim 24, it is similar in scope to claim 1 above and is rejected under the same rationale.

f. Regarding claim 26, it is similar in scope to claim 1 above and is rejected under the same rationale.

4. Claims 3, 4, 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al.

a. Regarding claim 3, Reynolds-Takasugi-Shreesha combination **does not disclose** correspondence between a data element being a pixel data in a frame of pixels, the frame having horizontal rows and vertical columns of pixels. Jones et al. **discloses** two dimensional image being organized in a two dimensional grid pattern of cells, each cell containing a matrix of pixels (col. 2, lines 3-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreesha

combination with the feature "multi-dimensional relationship between pixels" as taught by Jones et al. **because** it improves data access when retrieving these words associated with a dimensional image.

b. Regarding claim 4, Shreesha et al. **discloses** images containing 2048 x 2048 pixel values and other image sizes such as 2048 x 1536, 2048 x 1024 etc. (See col. 4, lines 65-67; table 1, col. 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to include 1920 x 1080 pixel as well **because** it provides for flexibility from the point of view of end-user who might prefer different image sizes depending on the application that is in use.

c. Regarding claim 12, Reynolds **discloses** a memory controller (memory controllers 41 and 42).

d. Regarding claim 22, it is similar in scope to claim 3 above and is rejected under the same rationale.

5. Claims 5-8 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al. as applied to claim 3 above and further in view of U.S. Patent No. 6,480,428 B2 to Zheng et al.

a. Regarding claims 5-8, Reynolds-Takasugi-Shreesha-Jones combination is **silent about** pixel data for pixels being stored/retrieved in one clock cycle using two memory devices for a pair of pixels and use of up to four memory devices

forming groups wherein these groups alternate between storing and retrieving pixel data. Zheng et al. **discloses** memory devices being arranged into a number of segment which supports access of multiple data bits within a single "active" clock cycle (...for a multi-bit memory access, two or more data bits may be retrieved from, or written to, two or more segments for each clock cycle...col. 4, lines 34-46). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreesha-Jones combination with the feature "accessing multiple data bits within a single "active" clock cycle" as taught by Zheng et al. **because** it provides for faster access to memory.

b. Regarding claim 25, it is similar in scope to claim 8 above and is rejected under the same rationale.

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al. as applied to claim 3 above and further in view of U.S. Patent No. 6,724,396 B1 to Emmot et al.

a. Regarding claims 13 and 14, Reynolds-Takasugi-Shreesha-Jones combination is **silent about** memory controller having two states for bank alteration wherein first state has pixel data stored in the first group of memory devices and pixel data is retrieved from the from the second group of memory devices and in the second state pixel data is retrieved from the first group of

devices and stored to the second group of memory devices. Emmot et al. **discloses** such an arrangement (...allocation of texture maps 210....is stored in consecutive blocks...left area 212*l* is allocated to consecutive blocks...in second memory area 244...and right area 212*r* is allocated to...in first memory area...similarly right area 212*r* ...right area...is allocated to first memory area...right area 214*r* is allocated to second memory area 244...in an alternating patterns...the memory allocation...avoids consecutive accesses to different pages in the same bank...col. 8, lines 21-67; col. 9, lines 1-67; col. 10, 1-67). Although Emmot et al. discloses texture map allocation, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreehsa-Jones combination with the feature "allocation of image date in this case pixels data which are "correlated data sets" among first and second memory areas" as taught by Emmot et al. **because** it reduces page miss penalty resulting in faster memory accesses.

7. Claims 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al. as applied to claim 1 above and further in view of U.S. Patent No. 5,668,568 to Holloman.

a. Regarding claim 16, Holloman **discloses** memory banks using three RAM groups with the possibility of additional RAM groups and logic associated with accessing these groups (col. 7, lines 1-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify

Reynolds-Takasugi-Shreehsa combination with the feature "three or more RAM groups" as taught by Holloman **because** it provides for storing larger images.

b. Regarding claim 17, Holloman **discloses** using low cost CMOS components operating below 40 megahertz. Therefore, it would have been obvious to use components operating at approximately 150 megahertz **because** it would result is faster memory operations.

c. Regarding claim 19, Reynolds **discloses** a memory controller (memory controllers 41 and 42).

d. Regarding claim 20, it is similar in scope to claim 16 above and is rejected under the same rationale.

8. Claims 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,150,679 to Reynolds in view of U.S. Patent No. 6,301,649 B1 to Takasugi, and further in view of U.S. Patent No. 6,496,192 B1 to Shreesha et al as applied to claim 1 above and further in view of U.S. Patent No. 6,018,354 to Jones et al. as applied to claim 3 above and further in view of U.S. Patent No. 6,724,396 B1 to Emmot et al. as applied to claim 13 above and further in view of U.S. Patent No. 5,668,568 to Holloman.

a. Regarding claim 15, Reynolds-Takasugi-Shreehsa-Jones-Emmot combination **is silent about** memory controller switching states based on a vertical synchronization signal. Holloman **discloses** such use where memory banks are switched based on vertical synchronizing pulse (col. 7, lines 1-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Reynolds-Takasugi-Shreehsa-Jones-Emmot with the feature "memory bank switching based on vertical sync pulse" as

taught by Holloman **because** it provides an efficient way to store/retrieve data from a memory bank.

Allowable Subject Matter

9. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-0377.

dks

September 30, 2004

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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